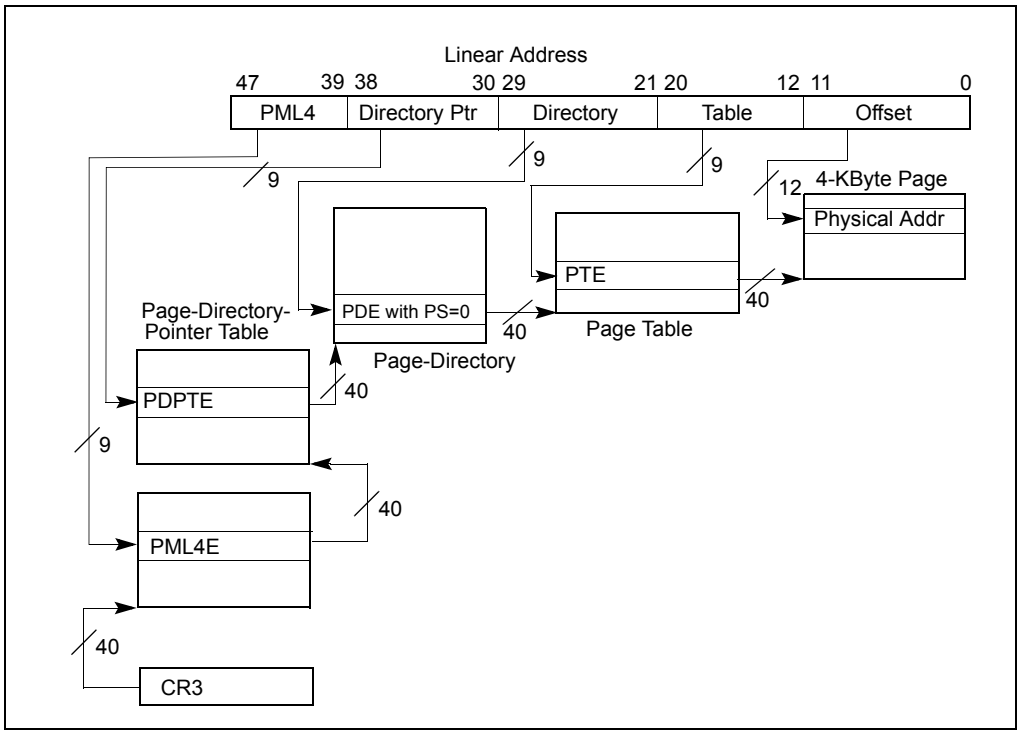

Figure 4-8. Linear-Address Translation to a 4-KByte Page using IA-32e Paging

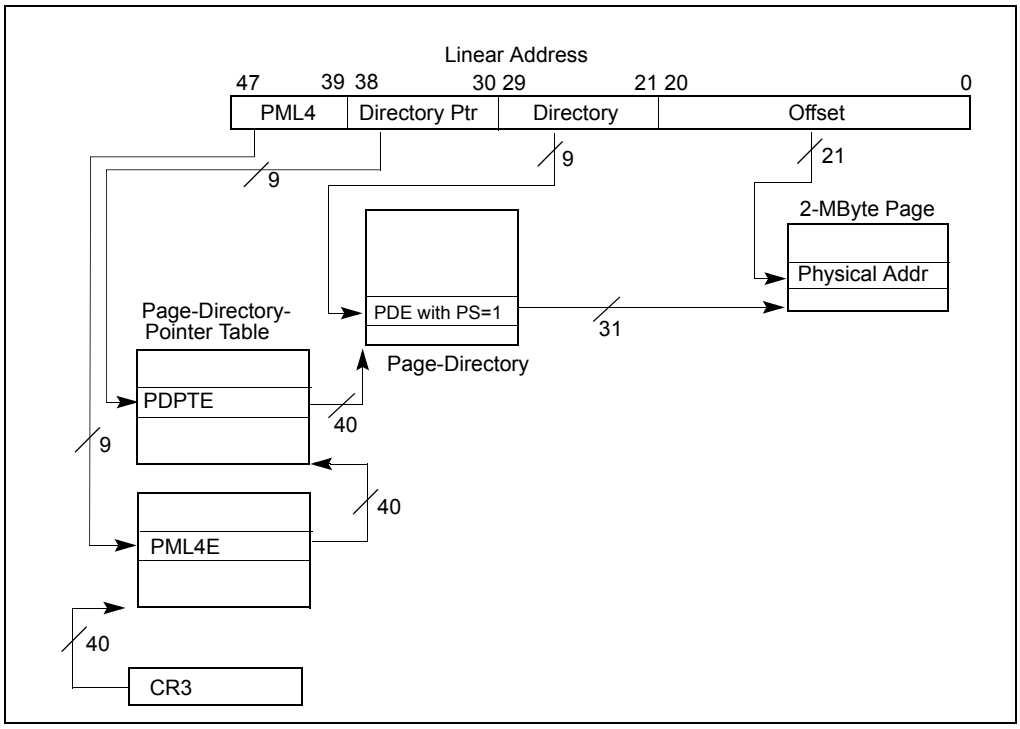

Figure 4-9. Linear-Address Translation to a 2-MByte Page using IA-32e Paging

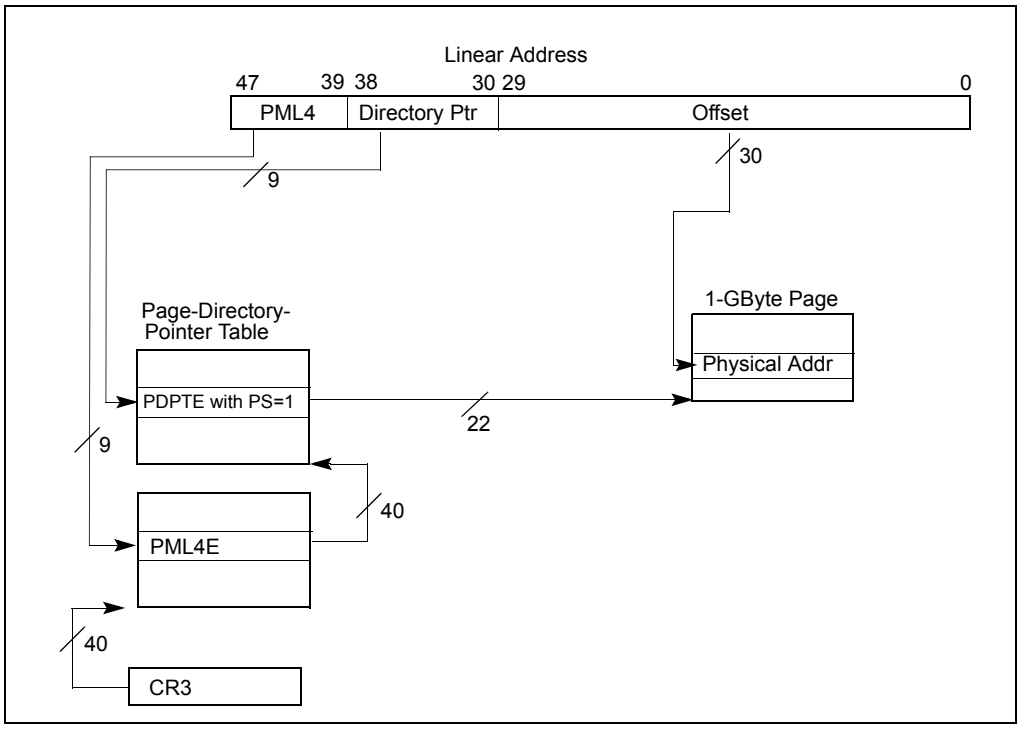

Figure 4-10. Linear-Address Translation to a 1-GByte Page using IA-32e Paging

The following items describe the IA-32e paging process in more detail as well has how the page size is determined.

- A 4-KByte naturally aligned PML4 table is located at the physical address specified in bits 51:12 of CR3 (see Table 4-12). A PML4 table comprises 512 64-bit entries (PML4Es). A PML4E is selected using the physical address defined as follows:
  - — Bits 51:12 are from CR3.
  - — Bits 11:3 are bits 47:39 of the linear address.
  - — Bits 2:0 are all 0.

  Because a PML4E is identified using bits 47:39 of the linear address, it controls access to a 512-GByte region of the linear-address space.
- A 4-KByte naturally aligned page-directory-pointer table is located at the physical address specified in bits 51:12 of the PML4E (see Table 4-14). A page-directory-pointer table comprises 512 64-bit entries (PDPTEs). A PDPTE is selected using the physical address defined as follows:
  - — Bits 51:12 are from the PML4E.