Multiple Preprocessing for Systematic SAT Solvers

Anbulagan and John Slaney

Logic and Computation Program, National ICT Australia (NICTA)

CSL, RSISE, The Australian National University

Canberra, Australia

Presented at IWIL-6, as part of LPAR-2006, Phnom Penh, Cambodia, 12 November 2006

SAT Problem

Input: A formula F in Conjunctive Normal Form (CNF)

Output: F is satisfiable by a consistent assignment of truth value to variables or F is unsatisfiable.

Example:

$$F = (x_1 \vee x_2 \vee x_3) \wedge (x_4 \vee \neg x_5) \wedge (\neg x_2 \vee x_6 \vee \neg x_7)$$

The first NP-Complete problem [Cook, 1971]

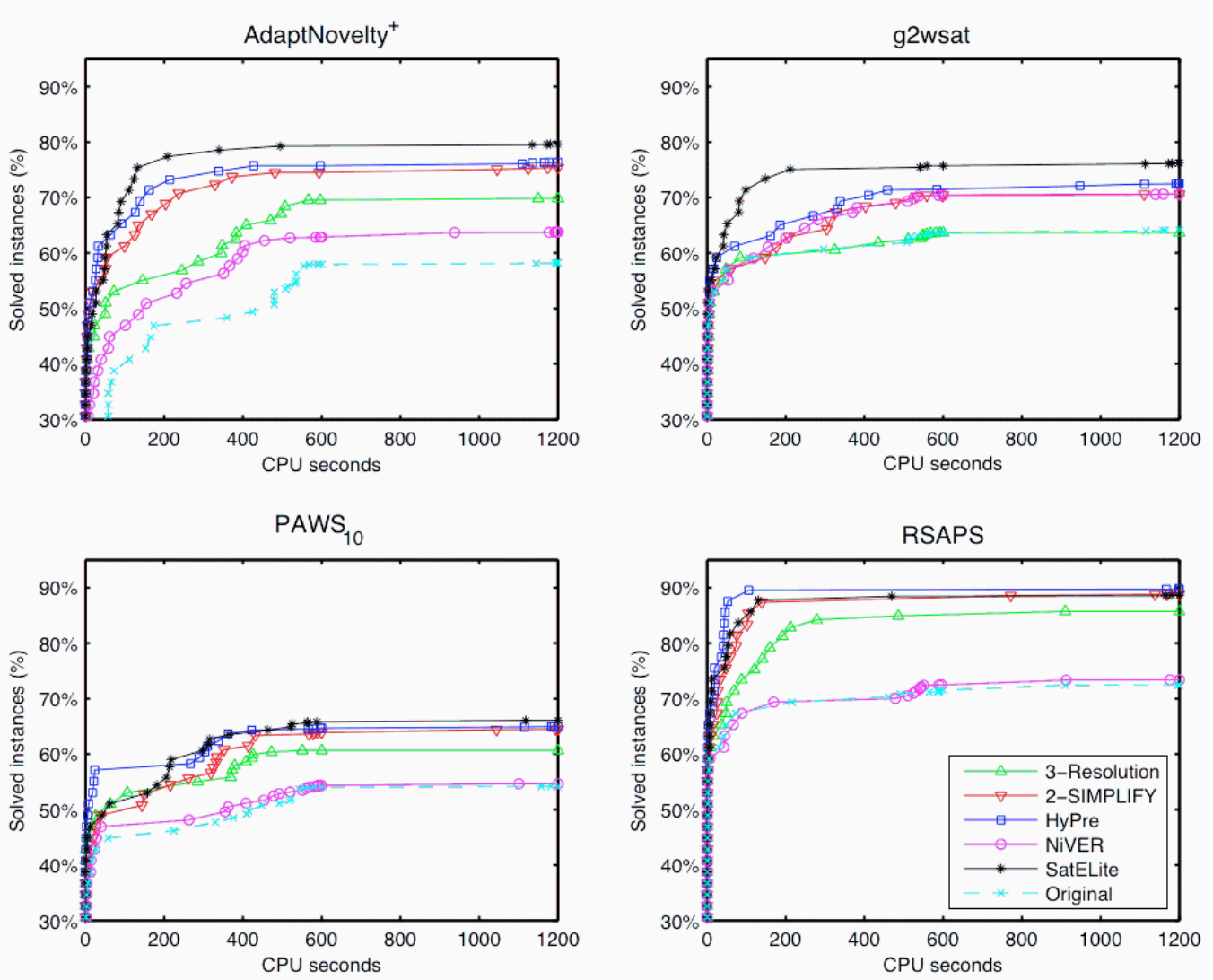
A central problem in mathematical logic, AI, and other fields of computer science and engineering.

Related Works

- The interaction between simplification and search in propositional satisfiability [Lynce and Marques-Silva, 2001]
  - Evaluate the impact of some preprocessors

- Boosting SLS performance by incorporating resolution-based preprocessor [Anbulagan *et al*., LSCS-2006]
  - Propose multiple preprocessing and preprocessor ordering

SLS Solvers: RTDs on Structured Problems



Multiple Preprocessing and Preprocessor Ordering

Using RSAPS (SLS solver)

Instances	Preprocessor	#Vars/#Cls/#Lits	Ptime	Succ. rate	CPU Time		Flips	
					median	mean	median	mean
ferry7-ks99i-	origin	1946/22336/45706	n/a	100	192.92	215.27	55, 877, 724	63, 887, 162
4001	SatELite	1286/21601/50644	0.27	100	4.39	5.66	897, 165	1, 149, 616
	HyPre	1881/32855/66732	0.19	100	2.34	3.26	494, 122	684, 276
	HyPre & Sat	1289/29078/76551	0.72	100	2.17	3.05	359, 981	499, 964
	Sat & HyPre	1272/61574/130202	0.59	100	0.83	1.17	83, 224	114, 180
ferry8-ks99i-	origin	2547/32525/66425	n/a	42	1, 200.00	910.38	302, 651, 507	229, 727, 514
4005	SatELite	1696/31589/74007	0.41	100	44.96	58.65	7, 563, 160	9, 812, 123
	HyPre	2473/48120/97601	0.29	100	9.50	19.61	1, 629, 417	3, 401, 913
	HyPre & Sat	1700/43296/116045	1.05	100	5.19	10.86	1, 077, 364	2, 264, 998
	Sat & HyPre	1680/92321/194966	0.90	100	2.23	3.62	252, 778	407, 258
par16-4	origin	1015/3324/8844	n/a	4	600.00	587.27	273, 700, 514	256, 388, 273
	HyPre	324/1352/3874	0.01	100	10.14	13.42	5, 230, 084	6, 833, 312
	SatELite	210/1201/4189	0.05	100	5.25	7.33	2, 230, 524	3, 153, 928
	Sat & HyPre	210/1210/4207	0.05	100	4.73	6.29	1, 987, 638	2, 655, 296
	HyPre & Sat	198/1232/4352	0.04	100	1.86	2.80	1, 333, 372	1, 995, 865

Resolution-based Preprocessors

- 3-Resolution [Li and Anbulagan, CP-1997]: computes resolvents for all pairs of clauses of length ≤ 3
- 2-SIMPLIFY [Brafman, IJCAI-2001]: constructs an implication graph from all binary clauses of a problem instance and uses a restricted variant of hyper-resolution.
- HyPre [Bacchus and Winter, SAT-2003]: reasons with binary clauses and do full hyper-resolution.
- NiVER [Subbarayan and Pradhan, SAT-2004]: Non increasing Variable Elimination Resolution.
- SatELite [Eén and Biere, SAT-2005]: improved NiVER with a variable elimination by substitution rule.

Preprocessor for Symmetry Detection

- Shatter [Aloul *et al*., DAC-2003]: detects symmetries and adds symmetry-breaking clauses. It increases the size of the formula.

Systematic SAT Solvers - Dew_Satz

- Based on Satz [Li and Anbulagan, IJCAI-1997]
  - A DPLL Procedure
  - Using Unit Propagation Look-Ahead (UPLA) based branching rule
- Some extensions:
  - Lookahead Saturation (LAS)
  - Neighbourhood Variable Ordering (NVO)
  - Dynamic Equality Weighting (DEW) during UPLA

Systematic SAT Solvers - MiniSat

- Conflict-driven clause learning (CDCL)
- Restart mechanism

Hard Structured Problems

- 32-bit Parity: one of ten challenges for SAT testing [Selman et al., IJCAI-1997]
- Ferry Planning: industrial problem at SAT2005 competition
- Bounded Model Checking (BMC)
  - BMC-IBM
  - BMC-galileo
  - BMC-alpha
  - IBM-FV-01
  - IBM-FV-26
- FPGA routing
- Original problem instance size
  - The smallest (FPGA-homer19) contains 330 variables and 2340 clauses
  - The largest (BMC-alpha-4408) contains 1,080,015 variables and 3,054,591 clauses

Empirical Study

- Time limit for each problem instance is 15000 seconds (4 hour and 10 minutes).
- On 16 AMD Athlon 64 processors running at 2.00GHz CPU with 2GB RAM.

Empirical Results on Parity and Planning

Instance	Prep.	#Var/#Cls/#Lits	Ptime	Dew_Satz		MiniSat	
				Stime	#BackT	Stime	#Conflict
par32-4	Orig	3176/10313/27645	n/a	>15000	n/a	>15000	n/a
	3Res	2385/7433/19762	0.08	10,425	10,036,154	>15000	n/a
	Sat	849/5160/18581	0.21	12,820	18,230,746	>15000	n/a
	Hyp+3Res	1331/6055/16999	0.36	9,001	17,712,997	>15000	n/a
	3Res+Hyp	1331/5567/16026	0.11	5,741	10,036,146	>15000	n/a
	Niv+3Res	1333/5810/16503	0.34	6,099	10,036,154	>15000	n/a
	3Res+Niv	1290/5297/15481	0.10	14,003	25,092,756	>15000	n/a
	3Res+Sat	850/5286/18958	0.35	3,552	7,744,986	>15000	n/a
	Sat+3Res	849/5333/19052	0.38	3,563	7,744,986	>15000	n/a
	Sat+2Sim	848/5154/18565	0.26	12,862	18,230,746	>15000	n/a
ferry10_ks99a	Orig	1977/29041/59135	n/a	>15000	n/a	0.03	710
	3Res	1955/28976/59017	0.13	>15000	n/a	0.03	827
	Hyp	1915/40743/82551	0.29	>15000	n/a	0.04	563
	Niv	1544/28578/58619	0.02	>15000	n/a	0.01	0
	Sat	1299/28246/66432	0.44	>15000	n/a	0.03	909
	2Sim	1945/27992/57049	0.05	>15000	n/a	0.05	1,565
	Sat+2Sim	1299/69894/149728	0.69	0.28	1	0.04	419
	3Res+2Sim+Niv	1793/21099/43369	0.43	0.08	0	0.06	1,278
	Niv+Hyp+2Sim+3Res	1532/24524/50463	0.54	5.19	3,949	0.02	454

Empirical Results on BMC

Instance	Prep.	#Var/#Cls/#Lits	Ptime	Dew_Satz		MiniSat	
				Stime	#BackT	Stime	#Conflict
BMC-IBM-12	Orig	39598/194778/515536	n/a	>15000	n/a	8.41	11,887
	Hyp	12205/87082/228241	92	>15000	n/a	0.74	1,513
	Niv	27813/168440/476976	0.69	>15000	n/a	4.46	8,702
	3Res	32606/160555/419341	2.77	>15000	n/a	6.77	10,243
	Sat	15176/109121/364968	4.50	>15000	n/a	2.37	6,219
	Niv+Hyp+3Res	12001/100114/253071	86	106	6	0.76	1,937
BMC-alpha-25449	Orig	663443/3065529/7845396	n/a	>15000	n/a	6.64	502
	Sat	12408/76025/247622	129	6.94	7	0.06	1
	Sat+Hyp	9091/61789/203593	566	7.82	2	0.10	109
	Sat+Niv	12356/75709/246367	130	4.48	2	0.06	1
	Sat+3Res	12404/77805/249192	130	8.84	1	0.06	1
	Sat+2Sim	10457/71128/229499	131	6.37	10	0.10	133
BMC-alpha-4408	Orig	1080015/3054591/7395935	n/a	>15000	n/a	5,409	587,755
	Sat	23657/112343/364874	47	>15000	n/a	1,266	820,043
	Sat+Hyp	13235/88976/263053	56	>15000	n/a	8,753	4,916,981
	Sat+Niv	22983/108603/351369	49	>15000	n/a	2,137	1,294,590
	Sat+3Res	23657/117795/380389	48	>15000	n/a	946	618,853
	Sat+2Sim	17470/129245/375444	52	>15000	n/a	804	561,529
	Sat+2Sim+3Res	16837/98726/305057	53	>15000	n/a	571	510,705

Empirical Results on IBM-FV

Instance	Prep.	#Var/#Cls/#Lits	Ptime	Dew_Satz		MiniSat	
				Stime	#BackT	Stime	#Conflict
IBM-FV-26-k90	Orig	444681/2250041/5877925	n/a	>15000	n/a	>15000	n/a
	Hyp	312101/2014169/5365681	446	>15000	n/a	1.55	583
	Niv	198605/1738024/5230908	6	>15000	n/a	1.38	429
	Sat	169470/1669436/6402318	140	>15000	n/a	8,240	3,311,629
	3Res	444681/2254141/5889005	195	27	1	1.26	10
	Niv+3Res	198605/2208074/6624608	121	13	1	1.77	5
	Hyp+3Res	312101/1979389/5187311	600	47	1	1.39	5

Empirical Results on FPGA Routing

Instance	Dew_Satz			MiniSat		
	#Solved	Stime	#BackT	#Solved	Stime	#Conflict
bart (21 SAT)	21	18	1,536,966	8	7,203	119,782,466
homer (15 UNSAT)	15	2,662	109,771,200	14	22,183	143,719,166

Instance	Prep.	#Var/#Cls/#Lits	Ptime	Dew_Satz		MiniSat	
				Stime	#BackT	Stime	#Conflict
bart-28	Orig	428/2907/7929	n/a	0	0	>15,000	n/a
	Sat	413/2892/11469	0.06	0.02	0	>15,000	n/a
	Sha	1825/8407/27003	0.37	0.06	9	198	775,639
	Sha+3Res	1764/7702/24400	0.46	0.04	1	2,458	7,676,459
	Sha+Hyp	1764/8349/26138	0.41	0.05	20	>15,000	n/a
	Sha+Niv	1781/8358/26759	0.38	0.05	6	5.46	53,683
	Sha+Sat	1728/8254/30422	0.53	0.10	0	115	684,272
	Sha+2Sim	1750/7892/24682	0.39	0.05	17	19.12	150,838
homer-20	Orig	440/4220/8800	n/a	941	19,958,400	>15,000	n/a
	Sat	400/4180/15200	0.08	1,443	6,982,425	11,448	57,302,582
	Sha	1999/10340/29988	0.28	369	350,610	1.83	22,950
	Sha+3Res	1907/8793/25027	0.37	362	405,059	1.41	18,273
	Sha+Hyp	1905/10527/29129	0.34	1,306	1,451,567	1.10	13,927
	Sha+Niv	1941/10276/29671	0.29	379	349,842	0.91	13,543
	Sha+Sat	1723/9420/30986	0.54	822	300,605	1.00	13,831
	Sha+2Sim	1879/9419/26188	0.31	114	120,297	0.40	6,612

Multiple Preprocessing and Preprocessor Ordering

Using Dew_Satz

Instance	Prep.	#Var/#Cls/#Lits	Ptime	Stime	#BackT
BMC-IBM-12	Hyp+3Res+Niv	10805/83643/204679	96.11	>15,000	n/a
	Niv+Hyp+3Res	12001/100114/253071	85.81	106	6
	3Res+Hyp+Niv	10038/82632/221890	89.56	>15,000	n/a
	3Res+Niv+Hyp	11107/99673/269405	58.38	>15,000	n/a
ferry10_ks99a	2Sim+Niv+Hyp+3Res	1518/32206/65806	0.43	>15,000	n/a
	Niv+3Res+2Sim+Hyp	1532/25229/51873	0.49	11,345	17,778,483
	3Res+2Sim+Niv+Hyp	1793/20597/42365	0.56	907	1,172,964
	Niv+Hyp+2Sim+3Res	1532/24524/50463	0.54	5	3,949
ferry10_ks99a	2Sim+Niv	1518/27554/56565	0.08	>15,000	n/a
	2Sim+Niv+2Sim	1518/18988/39433	0.27	3,197	6,066,241
	2Sim+Niv+ 2Sim+Niv	1486/18956/39429	0.29	129	290,871
	2Sim+Niv+ 2Sim+Niv+2Sim	1486/23258/48033	0.48	7,355	8,216,100

Conclusion

- High-performance SAT solvers benefit greatly from preprocessing.
- Improvements of four orders of magnitude in runtime are not uncommon.
- Multiple preprocessing can boost further the performance of SAT solvers.